R E M A R K S

The specification has been amended to address the objections in the Official Action. Additional editorial changes have been made so that the specification and drawing figures concur.

A proposed drawing correction is submitted herewith for Figures 2B, 4, 5A, 5B, 5C and 6.

Claims 1-6 were previously pending in the application and new claims 7-17 are added.

The original and new claims are believed patentable over the cited prior art for the following reasons.

MPEP 706.02(l)(1) states that effective November 29, 1999, subject matter that was prior art under 35 U.S.C. 103 via 35 U.S.C. 102(e) is disqualified as prior art against the claimed invention if the subject matter and the claimed invention "were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person."

MPEP 706.02(l)(2) states that "commonly owned" means wholly owned by the same person or organization at the time the claimed invention was made.

The present application is under assignment to NEC Corporation of Tokyo, Japan. SAKAO 6,184,584 lists NEC Corporation of Tokyo, Japan as the assignee. Applicant asserts that at the time the invention was made, SAKAO and

the present invention were commonly owned by NEC Corporation.

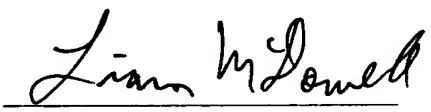
In addition, SAKAO was filed on April 14, 1999 and issued as a patent on February 6, 2001. The present application was filed on January 23, 2001. Since the present application was filed before SAKAO issued, then SAKAO would only be available under 35 U.S.C. 102(e). Therefore, Applicant believes that 35 U.S.C. 103 (c) applies to each claim in which SAKAO is used as a reference.

Accordingly, since SAKAO was applied against each of the original claims, and since new claims 7-17 include the subject matter of claims 1-6, claims 1-17 are believed patentable over the cited prior art. Reconsideration and allowance are respectfully submitted.

Attached hereto is a marked-up version of the changes made to the specification. The attached pages are captioned "Version With Markings To Show Changes Made."

Respectfully requested,

Young & Thompson

By 

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

Page 2, replace the paragraph beginning one line 5, as follows:

Regarding the multiple layered wiring, a structurally simple example is described with reference to [Fig. 5] Figures 5A-5C. Fig. 5A shows a method for directly connecting a first contact plug 24 and a second contact plug 26.

Page 2, replace the paragraph beginning on line 8, as follows:

As shown in Fig. 5A, on a semiconductor substrate 21, an element separating insulating film 22, a first interlayer insulating film 23, the first contact plug 24, a second interlayer insulating film 25, and the second contact plug 26 are arranged.

Page 3, replace the paragraph beginning on line 15, as follows:

Another example of the method shown in Fig. 5C using the contact plug is a conventionally known memory cell, that is, DRAM (Dynamic Random Access Memory) having a contact plug. An example of the cross-sectional structure of this type of memory cell is explained with reference to Fig. 6. In this structure, wiring for calling signals, which is

called a bit line or a signal line, is formed under the layer lower than the charge accumulation capacitor 60.

Page 3, replace the paragraph beginning on line 25, as follows:

A first interlayer insulating film 56 is formed so as to cover the element separating film 52 and the MOSFET. In order to connect the source-drain regions 51 and the first wiring layer formed on the first interlayer insulating film 56, polysilicon plugs 54 and 55 are formed. The bit wiring 57 on the first interlayer insulating film 56 is made of tungsten silicide. A second interlayer insulating film 58 [and a second contact plug 58 are] is formed so as to cover the bit wiring. A bottom electrode 59 of the capacitor is formed on the second interlayer, a capacitor dielectric film 60 is formed so as to cover the bottom electrode 59, and the upper layer of the capacitor dielectric film 60 is an upper electrode 61. The bottom electrode 59, the capacitor dielectric film 60, and the upper electrode 61 constitute a charge accumulation capacitor.--

Page 8, replace the paragraph beginning on line 1, as follows:

Figs. 2A to 2C are cross-sectional views showing the manufacturing process for a semiconductor device according to the [second] first embodiment of the present invention.

Page 8, replace the paragraph beginning on line 3, as follows:

Figs. 3A to 3C are cross-sectional views showing the manufacturing process for a semiconductor device according to the [third] first embodiment of the present invention.

Page 8, replace the paragraph beginning on line 5, as follows:

Fig. 4 is a cross-sectional view of a semiconductor device according to the [fourth] second embodiment of the present invention.

Page 9, replace the paragraph beginning on line 21, as follows:

Since the silicide pad 5, formed on the upper end surface of polysilicon plug 4, is disposed in a self-aligning manner, the silicide pad 5 is aligned on the polysilicon plug and there is [a] room to align the silicide pad on the tungsten plug 7, so that the connection between the silicide pad and the polysilicon plug 4 and the tungsten

plug 7 can be secured without concern for failure in connection.

Page 12, replace the paragraph beginning on line 23, as follows:

Subsequently, a BPSG film is formed at a thickness of 500 nm as the second interlayer insulating film 20 on the above formed films. The second contact hole is opened through the second interlayer insulating film 20 by conventionally known photolithography and the dry-etching process. A titanium nitride film is formed by spattering as a barrier layer between the adhered layer and silicon for forming the tungsten plug 21, and a tungsten layer 22 is formed by CVD for forming the second wiring.

Page 13, replace the paragraph beginning on line 8, as follows:

The manufacturing method of semiconductor devices according to one embodiment of the present invention determines the location of the silicide pads 5, 19 with respect to a polysilicon plug [18] 17 in a self-aligning manner. The above-described effects are thus obtained. Since the above-described process does not require masks for forming silicide pads 5 and 19, the length of the process can be reduced.